Docket No.: 03-2099 PATENT

UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Christopher Hamlin, et al.	:	By the Examiner:
Serial No.:	:	
Filed: January 29, 2004	:	Group Art Unit:

Title: METHOD AND APPARATUS FOR MAPPING PLATFORM-BASED DESIGN TO MULTIPLE FOUNDRY PROCESSES

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATION UNDER 37 C.F.R. §1.10

I hereby certify that this CIP Application Transmittal and the documents referred to as enclosed therein are being deposited with the United States Postal Service on this date, January 29, 2004 in an envelope as "Express Mail Post Office to Addressee", Mailing Label Nº EV 380 207 565 US, with sufficient postage, addressed to: MS Patent Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Penny L. Flint

Penny L. Flint DATED: January 29, 2004

Dear Sir:

INFORMATION DISCLOSURE STATEMENT

Applicant submits herewith patents, publications or other information of which he is aware, which he believes may be material to the patentability of this application and in respect of which there may be a duty to disclose in accordance with 37 CFR 1.56.

While this Information Disclosure Statement may be "material" pursuant to 37 CFR 1.56, it is not intended to constitute an admission that any patent, publication or other information referred to herein is "prior art" for this invention unless specifically designated as such.

In accordance with 37 CFR 1.97(g) the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR 1.56(a) exists.

The attached form, PTO-1449, provides a listing of patents, publications, or other information as required by 37 CFR 1.98(a)(1).

A copy of each of these items on PTO-1449 is supplied herewith.

Please direct all correspondence and telephone calls to:

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DATED: January 29, 2004.

Respectfully submitted,
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In Place of FORM PTO-1449 (Modified)	Serial No.:	
	Applicant:	Christopher Hamlin, et al.
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	Filing Date:	January 29, 2004
	Group:	
	Atty. Docket No.:	03-2099

Reference Designation

U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner Initial

____ AAA "Layout Compaction Accelerates SoC Design Through Hard IP Reuse," by Coby Zelnik, Senior Vice President, Business Development, Sagantec, Fremont, California, EE Times December 19, 2002 (10:47 a.m. EST); 3 pages; http://www.eetimes.com/story/OEG20021219S0026.

____ ABA "Layout Compaction in Digital Circuits," by Prof. Kurt Keutzer and A.R. Newton, EECS, University of California, Berkeley, CA; Implication of Deep Submicron, Simplex Solutions; © 1997, A. Richard Newton; 16 pages; www-cad.eecs.berkeley.edu/HomePages/keutzer/classes/ee244fa98/lectures/ee2443_2/ee2443_2.pdf.

____ ACA "Layout Compaction for Yield Optimization Via Critical Area Minimization," by Youcef Bourai and C.-J. Richard Shi, Electrical Engineering Department, University of Washington, Box 352500, Seattle, Washington 98195; 4 pages; http://jamaica.ee.pitt.edu/Archives/ProceedingArchives/Date/Date2000/papers/2000/date00/pdffiles/02c_4.pdf.

____ ADA "VLSI Layout Compaction Using Radix Priority Search Trees," by Andrew J. Harrison, March 12, 1991; 5 pages; Http://www.sigda.org/Archives/ProceedingArchives/Dac/Dac91/papers/1991/dac91/41_4/41_4.htm.

____ AEA "New Algorithms for Minimizing the Longest Wire Length During Circuit Compaction," by Susanne E. Hambrusch, Department of Computer Sciences, Purdue University, West Lafayette, IN 47907 and Hung-Yi Tu, Department of Computer Science and Information Management, Providence University, Taichung, Taiwan, ROC; January 26, 1995; 33 pages; http://www.cs.purdue.edu/homes/seh/papers/long-jour.pdf.

____ AFA "A Graph Based Simplex Method for the Integer Compaction Problem," by Alexey Lvov and Fook-Luen Heng, IBM Research; 1 page; http://researchweb.watson.ibm.com/compsci/algorithms/seminar.html.

____ AGA "Layout Synthesis Techniques for Yield Enhancement," by Venkat K.R. Chiluvuri and Israel Koren, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, MA 01003; 21 pages; http://citeseer.ist.psu.edu/cachedpage/90278/1. Originally published in *IEEE Trans. on Semiconductor Manufacturing*, Vol. 8, Special Issue on Defect, Fault, and Yield Modeling, pp. 178-187, May 1995.

Examiner: Date Considered:

EXAMINER: Initial if reference considered, whether nor not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.